Ordering number : ENN1792E

SANYO Semiconductors
DATA SHEET

2SK544 — N-Channel Silicon MOSFET
FM Tuner, VHF-Band Amplifier Applications

Features

- Low noise : NF=1.8dB typ (f=100MHz).
- High power gain : PG=27dB typ (f=100MHz).
- Small reverse transfer capacitance : Crss=0.035pF (V_{DS}=10V, f=1MHz).

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DS}		20	V
Gate-to-Source Voltage	V_{GS}		±5	V
Drain Current	I_D		30	mA
Allowable Power Dissipation	P_D		300	mW
Channel Temperature	Tch		125	°C
Storage Temperature	Tstg		−55 to +125	°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Voltage	V_{DSX}	V_{GS}=−4V, I_D=100μA	20			V
Gate-to-Source Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±5V			10	nA
Zero-Gate Voltage Drain Current	I_{DSS}*	V_{DS}=10V, V_{GS}=0V	1.2*		12*	mA
Cutoff Voltage	V_{GS}(off)	V_{DS}=10V, I_D=100μA			−2.5	V
Forward Transfer Admittance	|yfs|	V_{DS}=10V, V_{GS}=0V, f=1kHz		11		mS
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0V, f=1MHz		2.4		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, V_{GS}=0V, f=1MHz		0.035		pF
Power Gain	PG	V_{DS}=10V, V_{GS}=0V, f=100MHz, See Specified Test Circuit.		27		dB
Noise Figure	NF	V_{DS}=10V, V_{GS}=0V, f=100MHz, See Specified Test Circuit.		1.8	3.0	dB

* : The 2SK544 is classified by I_{DSS} as follows (unit : mA) :

Rank	D	E	F
I_{DSS}	1.2 to 3.0	2.5 to 6.0	5.0 to 125

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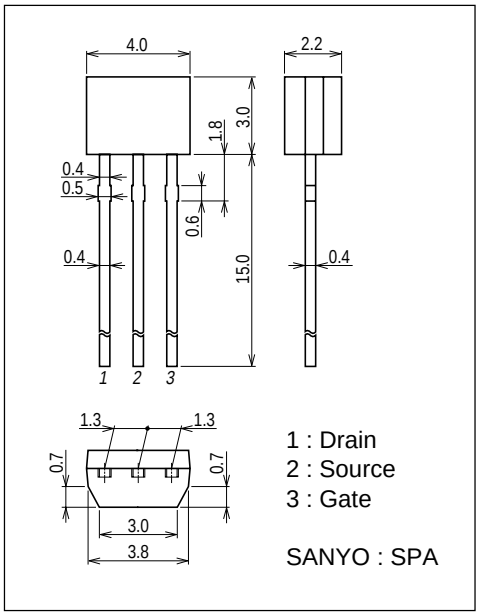
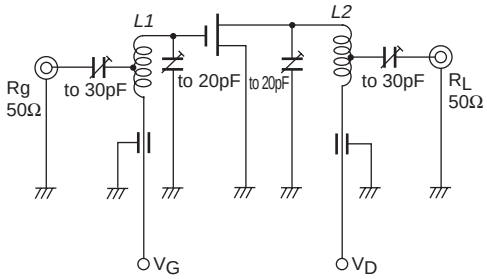
Package Dimensions

unit : mm

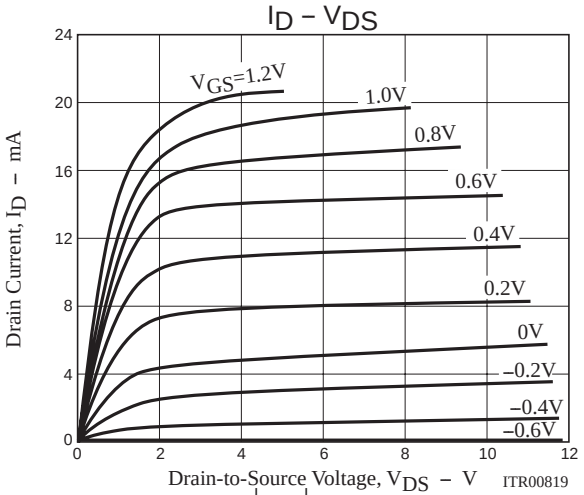
7524-006

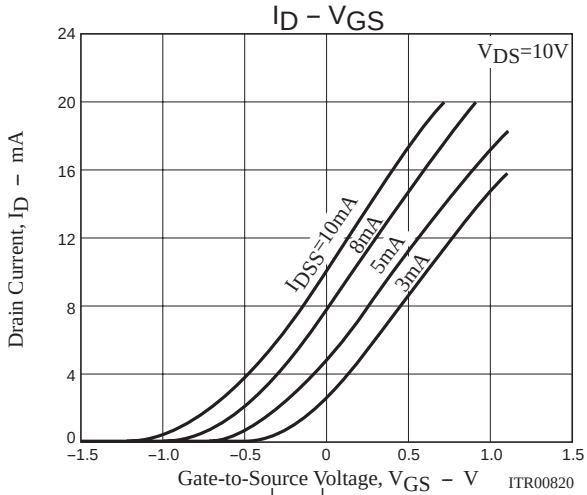


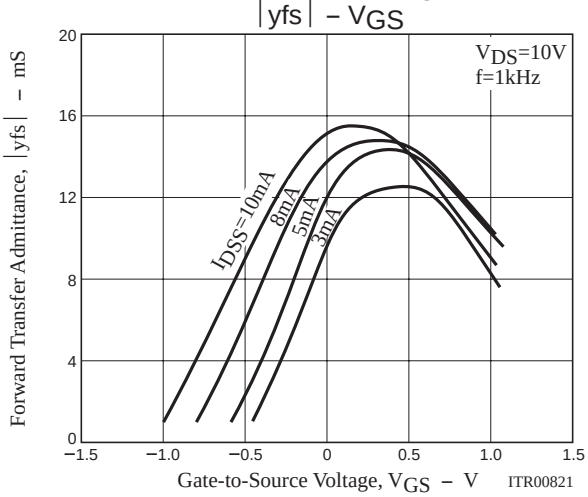
PG, NF Specified Test Circuit

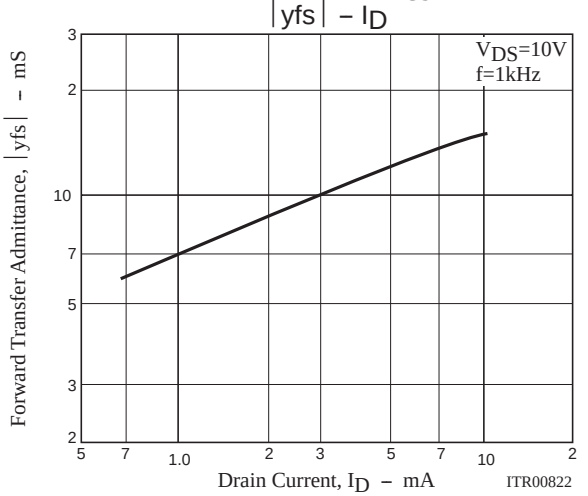


L1 : 1.0mmϕ plated wire 10mmϕ 6T, tap : 3T from H side
L2 : 1.0mmϕ plated wire 10mmϕ 7T, tap : 4T from H side

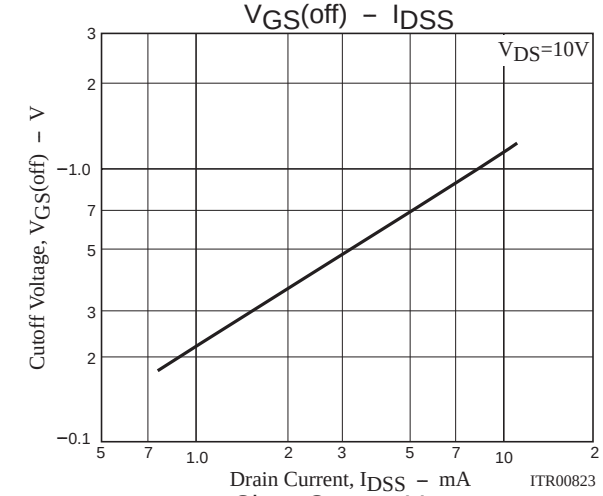




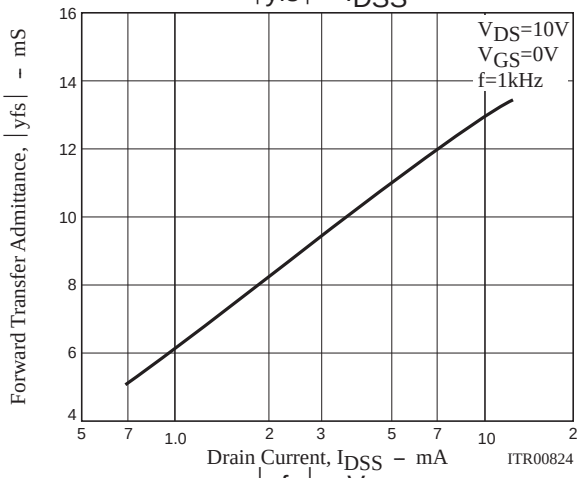




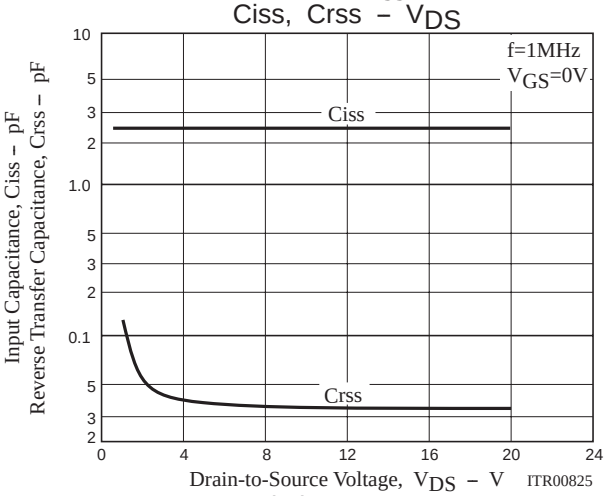
$V_{GS(off)}$ – I_{DSS}



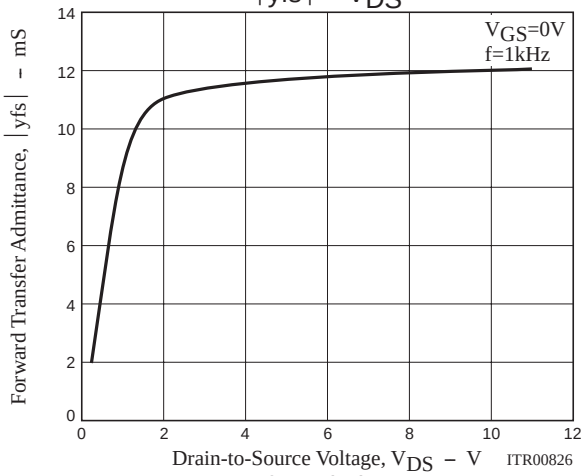
$|y_{fs}|$ – I_{DSS}



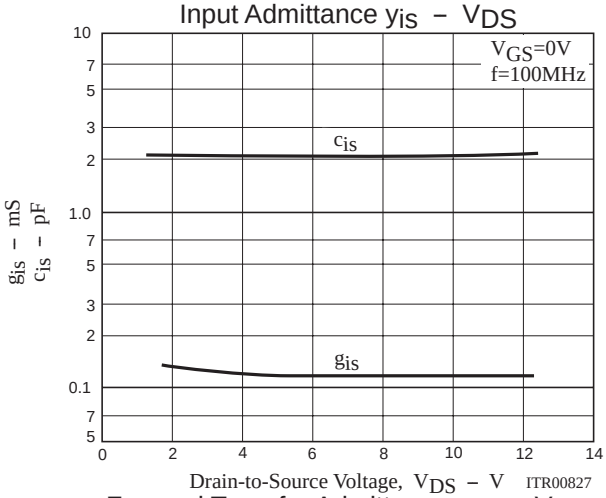
Ciss, Crss – V_{DS}



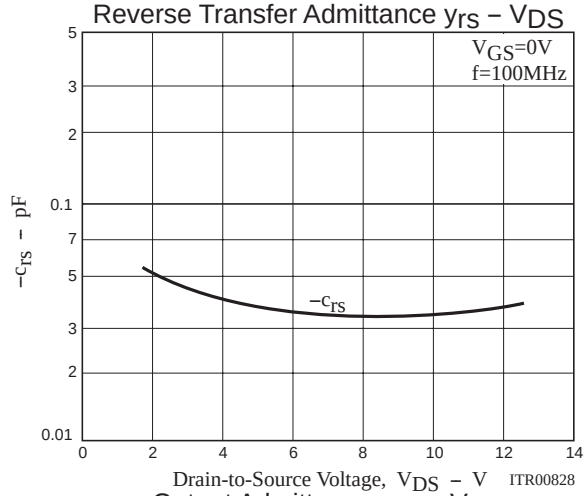
$|y_{fs}|$ – V_{DS}



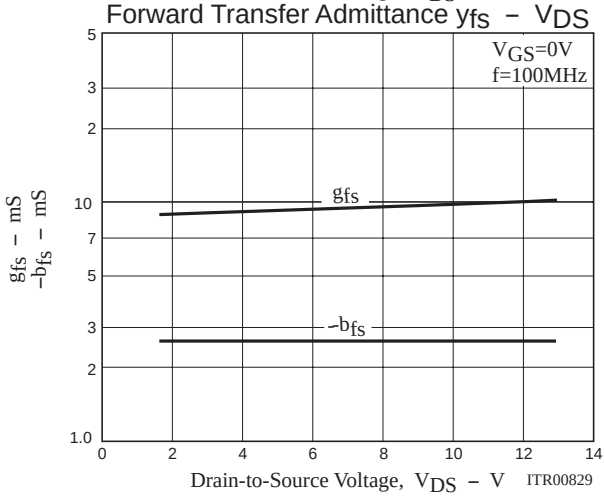
Input Admittance y_{is} – V_{DS}



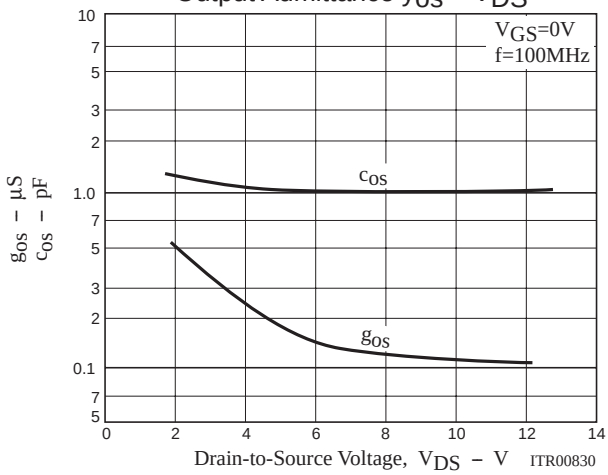
Reverse Transfer Admittance y_{rs} – V_{DS}



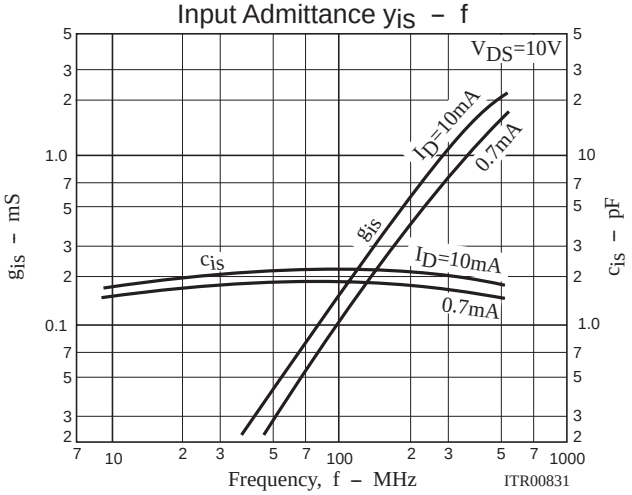
Forward Transfer Admittance y_{fs} – V_{DS}



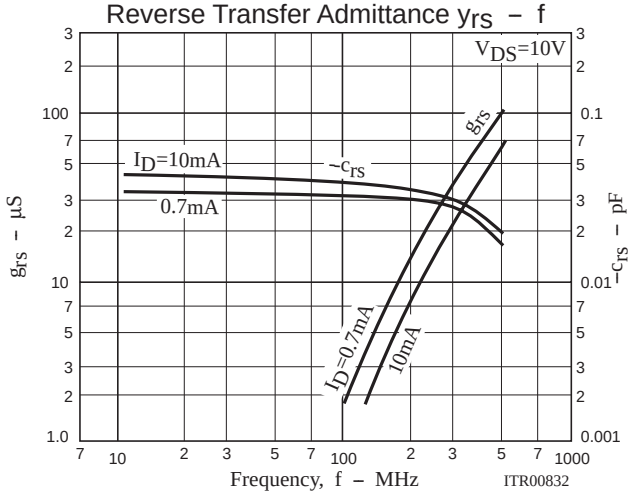
Output Admittance y_{os} – V_{DS}



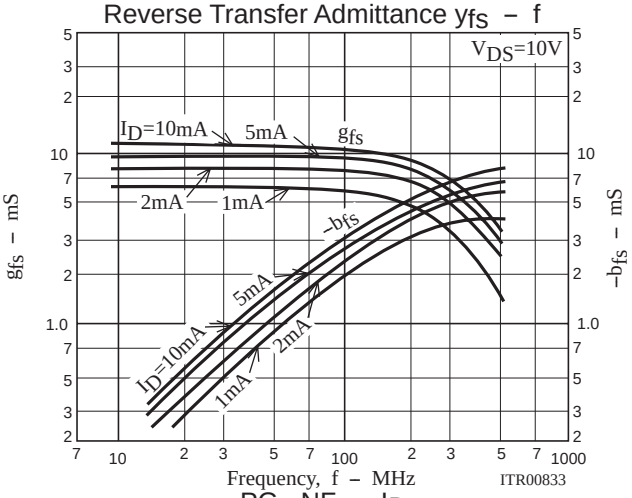
Input Admittance y_{is} – f



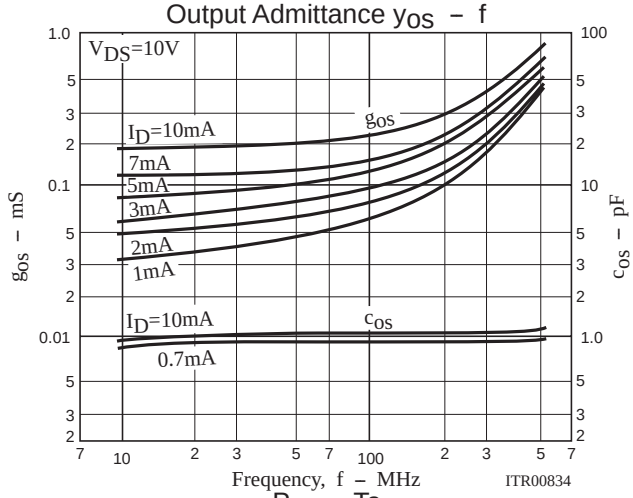
Reverse Transfer Admittance y_{rs} – f



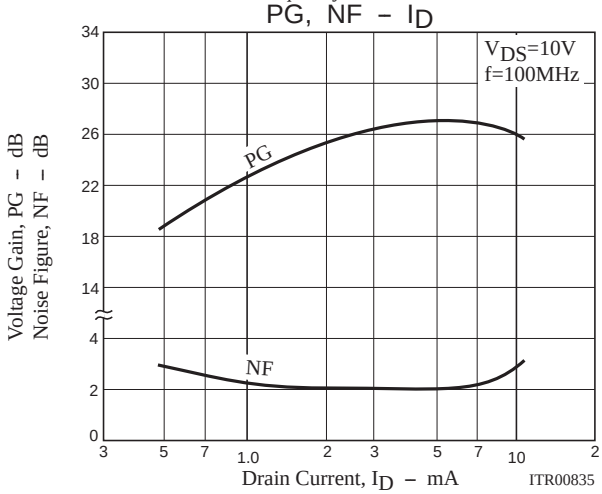
Reverse Transfer Admittance y_{fs} – f



Output Admittance y_{os} – f



PG, NF – I_D



P_D – Ta